AMENDMENTS TO THE CLAIMS

Please amend the claims as follows:

1. (currently amended) A method of making an electrically programmable memory element, comprising:

providing a first dielectric layer, said first dielectric layer having an opening, said opening having a sidewall surface and a bottom surface;

forming a conductive layer on said sidewall surface and on a portion of said bottom surface of said opening, said portion being less than the entire bottom surface;

forming a second dielectric layer ~~over~~ on said conductive layer, said second dielectric layer contacting said bottom surface of said opening; and

forming a programmable resistance material in electrical communication with said conductive layer.

Claims 2-6. (canceled)

7. (previously presented) The method of claim 1, wherein said programmable resistance material is a phase-change material.

8. (original) The method of claim 1, wherein said programmable resistance material includes a chalcogen element.

9. (original) The method of claim 1, wherein said first dielectric layer and said second dielectric layer are formed of the same material.

Claims 10-15. (canceled)

16. (previously presented) The method of claim 1, wherein said forming a conductive layer comprises conformally depositing said conductive layer.

17. (previously presented) The method of claim 1, wherein said forming a conductive layer comprises anisotropically etching said conductive layer.

18. (previously presented) The method of claim 1, wherein said programmable resistance material is electrically coupled to a top surface of said conductive layer.

19. (previously presented) The method of claim 1, wherein said conductive layer includes a conductive sidewall spacer.

20. (currently amended) A method of making an electrically programmable memory element, comprising:

providing a sidewall surface and an adjoining bottom surface;

forming a conductive layer on said sidewall surface and on a portion of said bottom surface, said portion being less than the entire bottom surface;

forming a dielectric material ~~over at least a portion of~~ on said conductive layer ~~and at least a portion of said bottom surface~~, said dielectric material contacting said bottom surface of said opening; and

forming a programmable resistance material in electrical communication with said conductive layer.

21. (previously presented) The method of claim 20, wherein said forming a conductive layer comprises conformally depositing said conductive layer.

22. (previously presented) The method of claim 20, wherein said forming a conductive layer comprises anisotropically etching said conductive layer.

23. (previously presented) The method of claim 20, wherein said programmable resistance material is electrically coupled to a top surface of said conductive layer.

Claim 24. (Canceled)

25. (previously presented) The method of claim 20, wherein said dielectric material is formed on said conductive layer before said forming a programmable resistance material.

26. (previously presented) The method of claim 20, wherein said sidewall surface is the sidewall surface of a dielectric layer.

Claims 27 and 28. (canceled)

29. (previously presented) The method of claim 26, wherein said dielectric material and said dielectric layer are formed of the same material.

30. (currently amended) A method of making an electrical device, comprising:

providing a sidewall surface and an adjoining bottom surface;

forming a conductive layer on said sidewall surface and on a portion of said bottom surface, said portion being less than the entire bottom surface;

forming a dielectric material ~~over at least a portion of~~ on said conductive layer, said dielectric material contacting said bottom surface of said opening ~~and at least a portion of said bottom surface~~; and

forming a chalcogenide material in electrical communication with said conductive layer.

31. (previously presented) The method of claim 30, wherein said forming a conductive layer comprises conformally depositing said conductive layer.

32. (previously presented) The method of claim 30, wherein said forming a conductive layer comprises anisotropically etching said conductive layer.

33. (previously presented) The method of claim 30, wherein said chalcogenide material is electrically coupled to a top surface of said conductive layer.

Claim 34. (canceled)

35. (previously presented) The method of claim 30, wherein said dielectric material is formed before said forming a chalcogenide material.

36. (previously presented) The method of claim 30, wherein said sidewall surface is the sidewall surface of a dielectric layer.

Claims 37 and 38. (canceled)

39. (previously presented) The method of claim 36, wherein said dielectric material and said dielectric layer are formed of the same material.

40. (previously presented) The method of claim 30, wherein said conductive layer includes a conductive sidewall spacer.

41. (currently amended) A method of making an electrical device, comprising:

forming an electrical contact by a method comprising:

providing a sidewall surface and an adjoining bottom surface,

forming a conductive layer on said sidewall surface and on a portion of said bottom surface, said portion being less than the entire bottom surface, and

forming a dielectric material ~~over at least a portion of~~ on said conductive layer ~~and at least a portion of said bottom surface~~, said dielectric material contacting said bottom surface of said opening; and

forming a chalcogenide material in electrical communication with said electrical contact.

42. (previously presented) The method of claim 41, wherein said forming a conductive layer comprises conformally depositing said conductive layer.

43. (previously presented) The method of claim 41, wherein said forming a conductive layer comprises anisotropically etching said conductive layer.

44. (previously presented) The method of claim 41, wherein said chalcogenide material is formed after forming said electrical contact.

45. (previously presented) The method of claim 41, wherein said electrical contact is a conductive sidewall spacer.

46. (previously presented) The method of claim 41, wherein said sidewall surface is the sidewall surface of a dielectric layer.

47. (currently amended) A method of making an electrical device, comprising:

forming an electrical contact by a method comprising:

providing a sidewall surface and an adjoining bottom surface,

forming a conductive layer on said sidewall surface and on a portion of said bottom surface said portion being less than the entire bottom surface; and,

forming a dielectric material ~~over at least a portion of~~ on said conductive layer ~~and at least a portion of said bottom surface~~, said dielectric material contacting said bottom surface of said opening; and

forming a phase-change material, in electrical communication with said electrical contact.

48. (previously presented) The method of claim 47, wherein said forming a conductive layer comprises conformally depositing said conductive layer.

49. (previously presented) The method of claim 47, wherein said forming a conductive layer comprises anisotropically etching said conductive layer.

50. (previously presented) The method of claim 47, wherein said phase-change material is formed after forming said electrical contact.

51. (previously presented) The method of claim 47, wherein said electrical contact is a conductive sidewall spacer.

52. (previously presented) The method of claim 47, wherein said sidewall surface is the sidewall surface of a dielectric layer.

53. (previously presented) The method of claim 47, wherein said phase-change material comprises at least one chalcogen element.

Claims 54-57. (canceled)

58. (previously presented) The method of claim 18, wherein said top surface of said conductive layer has a lateral dimension less than 1000 Angstroms.

59. (previously presented) The method of claim 20, wherein said portion of the bottom surface is a surface of a substrate.

60. (previously presented) The method of claim 20, wherein said conductive layer has an area of contact with said programmable resistance material, the area of contact having a dimension less than 1000 Angstroms.

61. (previously presented) The method of claim 20, wherein said forming a conductive layer comprises forming a dual-layered conductive sidewall spacer.

62. (currently amended) The method of claim 61, wherein said dual-layered conductive sidewall spacer comprises a first layer having a first resistivity and a second layer having a second resistivity, said first ~~resistiveity~~ resistivity being less than said second resistivity.

63. (previously presented) The method of claim 30, wherein a top surface of said conductive layer is in electrical communication with said chalcogenide material.

64. (previously presented) The method of claim 63, wherein said top surface has an area of contact with said chalcogenide material, the area of contact having a dimension less than 1000 Angstroms.

65. (previously presented) The method of claim 30, wherein said portion of the bottom surface is a surface of a substrate.

66. (previously presented) The method of claim 40, wherein said conductive sidewall spacer is a dual-layered conductive sidewall spacer.

67. (currently amended) The method of claim 66, wherein said dual-layered conductive sidewall spacer comprises a first layer having a first resistivity and a second layer having a second resistivity, said first ~~resistiveity~~ resistivity being less than said second resistivity.

68. (previously presented) The method of claim 41, wherein said portion of the bottom surface is a surface of a substrate.

69. (previously presented) The method of claim 41, wherein said conductive layer has an area of contact with said chalcogenide material, the area of contact having a dimension less than 1000 Angstroms.

70. (previously presented) The method of claim 41, wherein said forming a conductive layer comprises forming a dual-layered conductive sidewall spacer.

71. (currently amended) The method of claim 70, wherein said dual-layered conductive sidewall spacer comprises a first layer having a first resistivity and a second layer having a second resistivity, said first ~~resistiveity~~ resistivity being less than said second resistivity.

72. (previously presented) The method of claim 47, wherein said conductive layer has an area of contact with said phase-change material, the area of contact having a dimension less than 1000 Angstroms.

73. (previously presented) The method of claim 47, wherein said portion of the bottom surface is a surface of a substrate.

74. (previously presented) The method of claim 47, wherein said forming a conductive layer comprises forming a dual-layered conductive sidewall spacer.

75. (currently amended) The method of claim 74, wherein said dual-layered conductive sidewall spacer comprises a first layer having a first resistivity and a second layer having a second resistivity, said first ~~resistiveity~~ resistivity being less than said second resistivity.

76. (withdrawn) A method of fabricating an electrically operated memory array of programmable memory elements, comprising:

forming a cell area less than $8F^2$; and

utilizing three or less masking steps in addition to the number of masking steps used for a CMOS process flow.

77. (withdrawn) The method of claim 76, wherein one of said three or less masking steps is utilized prior to a deposition of a chalcogenide material.

78. (withdrawn) The method of claim 77, wherein said chalcogenide material is a phase-change memory material.

79. (withdrawn) The method of claim 76, wherein one of said three or less masking steps is utilized prior to a deposition of a dielectric material.

80. (withdrawn) A method of fabricating an electrically operated memory array of programmable memory elements, comprising:

forming a cell area less than $6F^2$; and

utilizing three or less masking steps in addition to the number of masking steps used for a CMOS process flow.

81. (withdrawn) The method of claim 80, wherein one of said three or less masking steps is utilized prior to a deposition of a chalcogenide material.

82. (withdrawn) The method of claim 81, wherein said chalcogenide material is a phase-change memory material.

83. (withdrawn) The method of claim 80, wherein one of said three or less masking steps is utilized prior to a deposition of a conductive material.

84. (withdrawn) A method of fabricating a non-charge-storage, electrically operated memory array, comprising utilizing three or less masking steps in addition to the steps used for a CMOS process flow.

85. (withdrawn) The method of claim 84, wherein the electrically operated memory array comprises a plurality of programmable memory elements.

86. (withdrawn) A method of fabricating a non-charge measurement, electrically operated memory array, comprising utilizing three or less steps in addition to the number of masking steps used for a CMOS process flow.

87. (withdrawn) The method of claim 86, wherein the electrically operated memory array comprises a plurality of programmable memory elements.

88. (new) The method of claim 1, wherein said conductive layer contacts said bottom surface of said opening.

89. (new) The method of claim 20, wherein said conductive layer contacts said bottom surface of said opening.

90. (new) The method of claim 30, wherein said conductive layer contacts said bottom surface of said opening.

91. (new) The method of claim 41, wherein said conductive layer contacts said bottom surface of said opening.

92. (new) The method of claim 47, wherein said conductive layer contacts said bottom surface of said opening.

93. (new) The method of claim 1, wherein said second dielectric layer fills said opening.

94. (new) The method of claim 20, wherein said dielectric material fills said opening.

95. (new) The method of claim 30, wherein said dielectric material fills said opening.

96. (new) The method of claim 41, wherein said dielectric material fills said opening.

97. (new) The method of claim 47, wherein said dielectric material fills said opening.